REMARKS

Claims 1-13 are pending in the above-identified application. Claims 1-13 were rejected. With this Amendment, claims 1,10 and 11 were amended to correct for typographical and cosmetic errors. In addition, new claim 14 was added that further distinguishes Applicants' invention. Accordingly, claims 1-14 are at issue.

I. 35 U.S.C. § 103 Obviousness Rejection of Claims 1-6 and 10

Claims 1-6 and 10 were rejected under 35 U.S.C. § 103(a) as being purportedly unpatentable over *Yang et al.* (US 6,468,894). Applicant respectfully traverses this rejection.

With respect to claim 1 and referring to Figures 5-6, 10A-12, 16A-18 as illustrative examples, Applicants claim a semiconductor device that has the following limitations:

a first buried wiring (105, 207, 316);

a second buried wiring (115, 216, 305) formed as a layer different from said first buried wiring (105, 207, 316);

a contact hole (108, 210, 308), which is formed between said first buried wiring (105, 207, 316) and said second buried wiring (115, 216, 305) and is filled with a wiring material electrically connecting said first buried wiring and said second buried wiring therethrough; and

a dummy hole (109, 203, 309), which has a hole diameter different from that of said contact hole (108, 210, 308), is so formed in the vicinity of said contact hole(108, 210, 308) so that a surface of said first buried wiring is exposed to said dummy hole (105, 207, 316), and is filled with a wiring material therein.

The Examiner argues that *Yang* teaches all the limitations of claim 1 except the limitation that the diameter of the dummy hole is different from that of the contact hole. The Examiner further argues that this limitation is obvious because diameters of via holes (contact and dummy) in the art of the semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired quality during fabrication. Applicants respectfully disagree.

Applicants teach that the problem of voids appearing in contacts (e.g., Copper vias) between buried wires as a result of stress migration (e.g., wiring and contacts subject to high temperature use for extended duration) may be solved by intentionally constructing a dummy hole extending to the first of the buried wires within proximity of the contact hole and having a different diameter than the contact hole such that stress migration is released by causing a void to appear or grow first (if at all) in the dummy hole rather than in the contact hole. *See* Application, at pg. 6 line 9 - pg. 8 line 1; pg. 26 line 1-pg. 27 line 6; pg. 33 line 5 - pg. 34 line 21; pg. 41 line 15 - pg. 42 line 21.

For example, with respect to the embodiment illustrated in Figures 5-6, Applicants teach (and claims in at least claims 2 and 10) that the dummy hole can be formed to have a diameter larger than the contact hole connecting a first and a second buried wiring when the dummy hole is formed in the vicinity of the contact hole over and in connection with the first buried wiring. Applicants further teach that when the dummy hole has a larger diameter than the contact hole, the etching rate of the dummy hole is greater relative to the concurrent etching rate of the contact hole such that the dummy hole is inevitably formed more deeply and has more etching damage than the contact hole. As a result, copper filed at the bottom of the dummy hole has weaker adhesion to the underlying first buried wiring than the copper filing the contact hole such that

subsequent stress migration of the first buried wiring and the contact hole is released by causing a void to first appear or grow in the dummy hole rather than in the contact hole. *See* Application, at pg. 20 line 24 - pg. 22 line 8; pg. 25 line 3 - pg. 26 line 21; Figs. 2B-5.

Alternatively, with respect to the embodiments illustrated in Figures 10A-12, and 16A-18, Applicants teach (and claim at least in claims 3-9 and 11-13) that the dummy hole can be formed to have a diameter smaller than the contact hole connecting a first and a second buried wiring when the dummy hole is formed in the vicinity of the contact hole so that a surface of the first buried wiring is exposed to the dummy hole. By forming the dummy hole to have a smaller diameter than the contact hole, Applicants further teach that the dummy hole may be formed to intentionally cause the dummy hole to have or generate a void such that subsequent stress migration of the first buried layer is released through the void in the dummy hole, preventing a void from forming in the contact hole. *See* Application, at pg. 27 line 18 - pg. 28 line 15; pg. 30 lines 10-16; pg. 33 line 5 - pg. 34 line 21; pg. 41 line 15 - pg. 42 line 21; Figs. 7B-11 & Fig. 14B-17.

In contrast, *Yang* teaches forming multiple redundant vias 30 with multiple dummy vias 32, 34, and 36 in the same dielectric material layer 18. The redundant vias 30 connect a first conductive line 14 in a first metal layer with a second conductive line 28 in a second metal layer but the dummy vias 32, 34, and 36 are either not connected to a conductive line (e.g., dummy via 32) or are connected to conductive lines other than the first conductive line 14 and the second conductive line 28 that the redundant vias 30 are connected. *See Yang*, Col. 5 lines 31-54; Fig. 7. Thus, *Yang* fails to teach the claim 1 limitation that "*a dummy hole ... is so formed in the vicinity of said contact hole so that a surface of said first buried wiring is exposed to said dummy hole.*"

Yang expressly discloses that the dummy vias 32, 34, and 36 are formed throughout the same dielectric material layer 18 to perform "only a mechanical strengthening function that helps to prevent delamination [of the vias from the dielectric material layer 18] and scratching during chemical mechanical polishing." *See Yang*, Col. 4 lines 42-47; Col. 5 lines 31-54. Accordingly, *Yang* teaches using dummy vias for a different purpose than Applicants claimed invention. In particular, *Yang* teaches forming redundant vias 30 in vicinity or proximity to each other and distributing dummy vias elsewhere within the same dielectric material layer 18 in order to strengthen the dielectric layer during chemical mechanical polishing.

As acknowledged by the Examiner, *Yang* also fails to teach the claim 1 limitation that the *"dummy hole [have] a hole diameter different from that of said contact hole is so formed in the vicinity of said contact hole to said first buried wiring."* The Examiner argues that this limitation is obvious in view of *Yang* "as diameters of via holes (contact and dummy) in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired quality during fabrication." Applicants respectfully disagree.

Applicants submit that in the art of semiconductor manufacturing contact holes are typically optimized to provide the smallest footprint or profile in association with a buried wiring. Applicants further submit that this optimization leaves the contacts susceptible to the problem identified by the Applicants, namely the potential of a void formation in the contact due to stress migration of the buried wiring. See Application, at pgs. 3-4.

Applicants' solution to this problem as claimed is not obvious. As discussed above, Applicants teach that a contact formed between a first buried layer and a second buried layer may be protected from the formation of a void due to stress migration of the first buried layer

(which may occur during use after fabrication) by forming a dummy hole to have a diameter different than the contact hole, where the dummy hole is disposed in the vicinity of the contact hole so that the dummy hole connects to the first buried layer. Moreover, by forming redundant vias 30 of the same diameter to connect to a specific conductive line, *Yang* teaches away from Applicants claimed invention as each of the redundant vias 30 are susceptible to the formation of a void when the conductive line is subjected to stress migration.

Accordingly, *Yang* (alone or in combination with any prior art cited by the Examiner) fails to teach or suggest all the claim 1 limitations. Accordingly, Applicants respectfully request that the rejection to claim 1 be with drawn.

Claims 2-6 depend directly or indirectly from claim 1 and should be deemed allowable for at least the same reasons as claim 1.

Claim 10 is directed to a method for manufacturing a semiconductor device having limitations similar to claim 1 and 2 as discussed above. Accordingly, Applicants respectfully request that the rejection to claim 1 be withdrawn for at least the same reasons as claim 1.

II. 35 U.S.C. § 103 Obviousness Rejection of Claims 7-9 and 11-13

Claims 7-9 and 11 were rejected under 35 U.S.C. § 103(a) as being purportedly unpatentable over *Yang* as applied to claims 1-6 and 10, and further in view of prior art of the instant application. Claims 12 and 13 were rejected under 35 U.S.C. § 103(a) as being purportedly unpatentable over *Yang* in view of *Yamaha et al.* (US 5,885,857) and Prior Art of the instant application. Applicant respectfully traverses these rejections.

Claims 7-9 depend directly or indirectly from claim 1 and should be deemed allowable for at least the same reasons as claim 1.

Claim 11 is directed to a method for manufacturing a semiconductor device having limitations similar to claims 1, 3, and 7 as discussed above. Accordingly, Applicants respectfully request that the rejection to claim 11 be withdrawn for at least the same reasons as claim 1.

Claim 12 is directed to a method for manufacturing a semiconductor device having limitations similar to claims 1, 4, and 8 as discussed above. Accordingly, Applicants respectfully request that the rejection to claim 12 be withdrawn for at least the same reasons as claim 1.

Claim 13 is directed to a method for manufacturing a semiconductor device having limitations similar to claims 1, 5, and 9 as discussed above. Accordingly, Applicants respectfully request that the rejection to claim 13 be withdrawn for at least the same reasons as claim 1.

Moreover, with respect to claim 7, Applicants claim a semiconductor device that has, among other limitations, a dummy hole having a diameter smaller than the contact hole and "so set as to cause a plugging failure when [the] dummy hole is filled with said wiring material." Claims 8-9 and 11-13 have similar limitations.

The Examiner acknowledges that *Yang* does not disclose that a plugging failure is caused by "filing the dummy hole of a selected size [smaller than the contact hole] with wiring material." However, the Examiner argues that the background section of the instant application teaches this limitation. Applicants respectfully disagree.

As discussed above, Applicants submit that the optimization of contact size or footprint leaves the contacts susceptible to the problem identified by the Applicants in the background section, namely the potential of a void formation in the contact due to stress migration of the

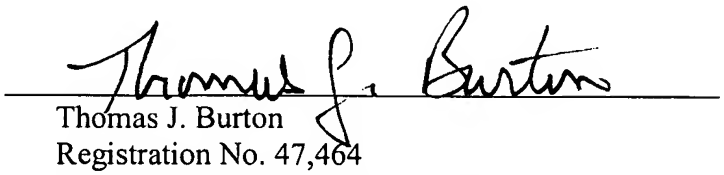
buried wiring. See Application, at pgs. 3-4. The background section, however, does not discuss forming a dummy hole to have a smaller diameter in relation to a contact hole so that when the dummy hole is filled it has an intentionally formed void. Applicants teach that this intentionally formed void functions to prevent the subsequent formation of a void in a contact hole due to stress migration of the buried wiring connecting the contact hole and the dummy hole.

Thus, Applicants submit the background section does not teach the limitation of forming a dummy hole having a diameter smaller than the contact hole and so set as to cause a plugging failure when the dummy hole is filled with said wiring material. Accordingly, Applicants submit that none of the cited prior art references, alone or in combination with the background section, teach or suggest all the limitations of claims 7-9 and 11-13 and respectfully request that the rejection of these claims be withdrawn for this additional reason.

III. Conclusion

In view of the above amendments and remarks, Applicant submits that all claims are clearly allowable over the cited prior art, and respectfully requests early and favorable notification to that effect.

Respectfully submitted,

Dated: August 19, 2005 By: 

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